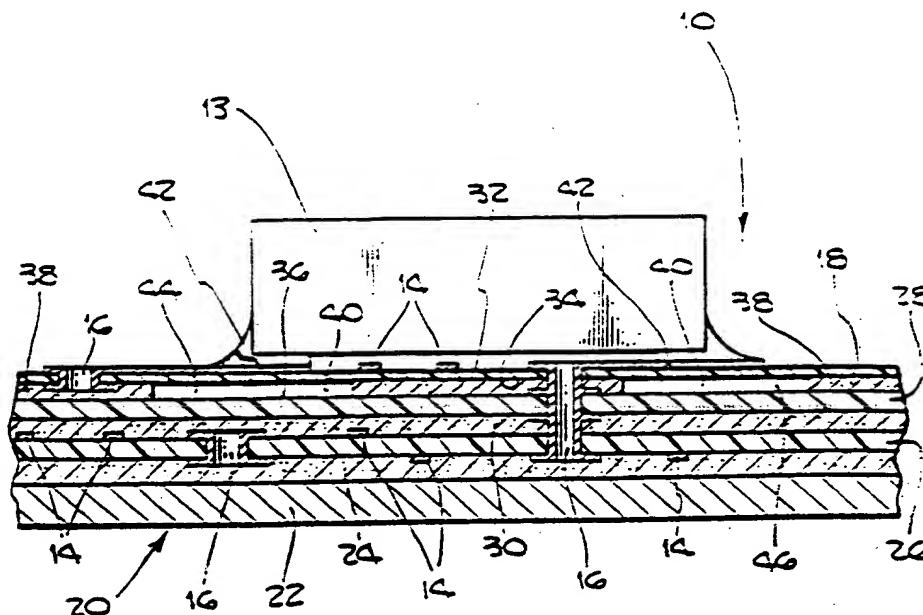




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁴ :		A1	(11) International Publication Number: WO 89/0953
H05K 1/18			(43) International Publication Date: 5 October 1989 (05.10.89)
(21) International Application Number: PCT/US88/04516		(74) Agents: LACHMAN, Mary, E. et al.; Hughes Aircraft Company, P.O. Box 45066, Building C1, M.S. A12, Los Angeles, CA 90045-0066 (US).	
(22) International Filing Date: 16 December 1988 (16.12.88)		(81) Designated States: DE (European patent), DK, FF (European patent), GB (European patent), JP, NL (European patent).	
(31) Priority Application Numbers: 171,047 171,048		Published	
(32) Priority Dates: 21 March 1988 (21.03.88) 21 March 1988 (21.03.88)		With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.	
(33) Priority Country: US			
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(54) Title: THERMAL EXPANSION MISMATCH FORGIVABLE PRINTED WIRING BOARD FOR CERAMIC LEADLESS CHIP CARRIER



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THERMAL EXPANSION MISMATCH FORGIVABLE PRINTED
WIRING BOARD FOR CERAMIC LEADLESS CHIP CARRIERBACKGROUND OF THE INVENTION5 1. Field of the Invention

The present invention relates generally to the surface mounting of ceramic leadless chip carriers to printed wiring boards. More particularly, the present invention relates to methods and apparatus for increasing the reliability of the solder joint integrity between the printed wiring board and the chip carrier.

15 2. Description of Related Art

The surface mounting of electronic devices, such as ceramic leadless chip carriers, has become popular due to the ability to save weight and volume in electronic equipment when such surface-mount technology is used. In addition, the need for increased circuit density makes surface mounting of chip carriers even more desirable.

20 Typically, the ceramic leadless chip carrier is mounted to the printed wiring board surface by way of solder fillets or joints. It is important that the integrity and reliability of the solder joint be maintained for long periods of time and be able to withstand numerous temperature and power cycles. In addition, the solder joint must be able to withstand shock and vibration which may occur in many electronic systems such as those used in avionics.

25 The increasing popularity of surface mounting of ceramic leadless chip carriers has brought with it

concerns over the reliability and integrity of the solder joints between the chip carriers and the printed wiring board. Cracking and other disturbances to the joint integrity have been noted. Joint cracking is believed to be due mainly to differences in the thermal coefficients of expansion between the printed wiring board and the chip carriers. Various different approaches have been taken to reduce the possibility of solder joint cracking. These approaches have included making the printed wiring board out of materials having thermal coefficients of expansion which are close to the thermal coefficient of expansion for the ceramic leadless chip carriers. In addition, attempts have been made to replace the solder joint with a joint which is less likely to crack, such as electrically conductive epoxy compounds. Although the various approaches used to date have experienced different degrees of success, there still is a continuing need to provide a method for surface mounting ceramic leadless chip carriers to printed wiring boards wherein the possibility of solder joint cracking is eliminated.

SUMMARY OF THE INVENTION

The present invention provides an improved method and apparatus for mounting ceramic leadless chip carriers to printed wiring boards wherein the chances of solder joint cracking are reduced to thereby increase the reliability and integrity of the system.

The present invention is based upon fabricating the printed wiring circuit board so that the top layer of the board expands and contracts with the chip carrier regardless of the expansion or contraction rates of the main body of the wiring board.

The printed wiring board in accordance with the present invention includes an expansion layer having a bottom surface and top surface wherein the top surface

of the expansion layer forms the top surface of the printed wiring board. The expansion layer is supported by a rigid support layer which also has a top and a bottom. The bottom of the expansion layer is bonded to the top of the rigid support layer except in the area located directly below the footprint of the chip carrier and solder joints. This lack of bonding between the expansion layer and rigid support layer provides a forgivable expansion area located underneath the chip carrier footprint wherein the expansion layer can expand and contract the same amount as the chip carrier irrespective of the expansion and contraction rates of the rigid support layers.

As a feature of the present invention, the expansion layer is relatively thin and flexible, and the leadless chip carrier solder joint stress caused by thermal expansion mismatch between the leadless chip carrier and the expansion layer is extremely low so that the chances for solder joint cracking are reduced.

As a feature of the present invention, a polytetrafluoroethylene (PTFE) dispersion or emulsion is applied onto the bottom of the expansion layer at those locations where bonding is not desired. The PTFE dispersion is then dried and cured to form non-bonding areas. Subsequent bonding of the expansion layer to the rigid support layer provides bonding everywhere except at the non-bonding locations provided by the PTFE layer.

Conventional mold release systems do not work well with the adhesives (such as polyimide prepreg) that are typically used to bond layers together in laminated circuit boards. The PTFE aqueous dispersion, on the other hand, works well with many adhesives. The cured PTFE layer also will survive the vapor phase soldering condition which is a required step in the component placement operation. In addition, the use of a cured

PTFE dispersion as the release agent is cost effective and can be easily adapted to high volume production.

The above-described and many other features and attendant advantages of the present invention will become better understood by reference to the following description when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

10 In the accompanying drawings:

FIG. 1 is a perspective view of a printed wiring board prior to mounting of the ceramic leadless chip carriers.

15 FIG. 2 is a cross-sectional view of the printed wiring board with a leadless ceramic chip carrier soldered thereon in accordance with a first embodiment of the present invention.

20 FIG. 3 is a cross-sectional view of the printed wiring board with a leadless ceramic chip carrier soldered thereon in accordance with an alternative embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred printed wiring board in accordance with the present invention is shown generally at 10 in FIGS. 1, 2 and 3. The printed wiring board 10 is shown in FIG. 1 prior to mounting of the ceramic leadless chip carriers. The board 10 includes a plurality of chip carrier mounting pads 12. Circuit lines connecting the various circuitry are shown at 14. Via holes are shown at 16. The circuit lines and via holes are provided for illustration purposes only since these are conventional features of any printed wiring board and do not form a part of the invention. A detailed sectional view of a portion of the printed wiring board 10 is shown in FIG.

2 after the ceramic leadless chip carrier 13 is mounted thereon.

The preferred printed wiring board includes an expansion layer 18 which is bonded to a rigid support 5 layer shown generally at 20. The support layer 20 is a multi-layer laminated board, which as best shown in FIG. 2, includes a metal plate 22, thermally conductive adhesive layer 24, and polyimide impregnated glass fiber layers 26 and 28 (referred to herein as polyimide fiberglass) which are bonded together by adhesive layer 30. The metal plate 22 is optional. As is well known, metal 10 plates are included as part of a printed wiring board where it is desirable to thermally conduct heat away from the printed wiring board and where added strength 15 is desired. If a metal plate 22 is used, it is desirable to use a thermally conductive adhesive 24 in order to ensure that heat from the printed wiring board is conducted to the metal plate 22.

The polyimide fiberglass layers 26 and 28 do not 20 necessarily have to be made of polyimide fiberglass. Other suitable printed wiring board materials, such as epoxy fiberglass, polyimide quartz fibers, alumina (ceramic) fiber substrates, polyimide aramid fibers and any other suitable composite materials typically used in 25 printed wiring boards can also be used as the printed wiring board layers. The adhesive layer 30 which is used to bond the layers 26 and 28 together may also be any of the conventionally known adhesives commonly used in preparing laminated printed wiring boards. Examples 30 of suitable adhesives include epoxy prepreg, polyimide prepreg, etc.

When a metal layer 22 is used, it will preferably have a thickness of between about 0.030 inch (0.076 cm) 35 to 0.300 inch (0.76 cm), most preferably between about 0.050 inch (0.13 cm) to 0.300 inch (0.76 cm). The polyimide fiberglass layers 26 and 28 preferably have

thicknesses of between about 0.004 inch (0.010 cm) to 0.25 inch (0.64 cm), most preferably to 0.090 inch (0.23 cm). The thickness of the two adhesive layers 24 and 30 are preferably between about 0.004 inch (0.010 cm) to 5 0.012 inch (0.030 cm). The particular metal used for the metal layer can be any of those conventionally used in printed wiring boards including aluminum, copper and copper alloys and any other suitable thermally conductive metal.

10 In conventional printed wiring boards, the ceramic leadless chip carrier would be attached directly to the laminated support layer 20. However, in accordance with the present invention, an expansion layer 18 is provided. The expansion layer 18 includes a top 32 and bottom 34. The bottom 34 of expansion layer 18 is bonded to the top 36 of the support layer 20 by way of adhesive layer 38. As best shown in FIG. 2, the adhesive layer 38 is not bonded to the expansion layer 18 underneath the chip carrier 13. This leaves an unbonded area 40 where the expansion layer 18 is not attached to the support layer 20. This provides an expansion area wherein the expansion layer 18 is free to expand and contract with chip carrier 13 irrespective of the remainder of the printed wiring board 20. In an alternative embodiment of the present invention, as shown 15 in FIG. 3, and discussed below, a layer of polytetra-fluoroethylene (PTFE) 39 is provided which prevents adhesion of the support layer 20 to the expansion layer 18.

20 As shown in FIGS. 2 and 3, the chip carrier 13 is mounted onto the top 32 of expansion layer 18 by way of solder fillets or joints 42. The area under the chip carrier 13 and solder joints 42 is defined as the footprint of the chip carrier. In accordance with the 25 present invention, the adhesive layer 38 provides no bonding at locations beneath the chip carrier footprint.

The area of non-bonding will extend slightly outward from the footprint as best shown at 44 and 46 in FIG. 2. This provides a non-bonded portion of the expansion layer 18 which does not lie directly beneath the chip carrier footprint. 5 It is essential that this extra non-bonded portion be provided.

The expansion layer 18 is made from a material having low modulus of elasticity, such as a polyimide film. A preferred polyimide film is marketed by E. I. 10 DuPont under the trade name KAPTON. Other flexible films are possible so long as they have properties similar to polyimide including high temperature stability and good bonding characteristics. These films should not contain fillers, such as glass particles or beads 15 which might adversely affect the flexibility of the film.

The thickness of the expansion layer should be such that it has some degree of flexibility while still being structurally strong. Layer thicknesses of between 20 0.0005 inch (0.001 cm) to 0.005 inch (0.013 cm) are suitable. Suitable adhesives for attaching the expansion layer 18 to the support layer 20 include no-flow type adhesives such as polyimide prepreg, epoxy prepreg, etc. The thickness of the adhesive layer should be less 25 than about 0.10 inch (0.25 cm).

Polyimide films are preferred for use as the expansion layer because polyimide sheeting can be made in very thin sheets while being structurally strong. Further, the modulus of elasticity for polyimide films 30 are very low (4.6×10^5 psi). Accordingly, the stretching or shrinking of the thin expansion layer under the chip carrier will cause very low stress on the solder joints 42. This stress will be substantially below the fatigue stress of the solder joint. Therefore, the 35 solder joint will not develop cracks.

Any suitable fabrication technique can be utilized in order to insure that the expansion layer 18 is not bonded to the top 36 of support layer 20 at locations under the chip carrier footprint. For example, the 5 unbonded footprint area 40 can be achieved by die cutting the prepreg adhesive layer or by applying various mold release agents on the bottom 34 of expansion layer 18 to prevent the adhesive 38 from adhering to the area below the chip carrier. In addition, layers or sheets of conventional release materials may be inserted between the expansion layer bottom 34 and the top 36 of support layer 20.

In accordance with an alternative embodiment of the present invention, the unbonded footprint area 40 is 15 provided by applying a thin layer of an emulsion of polytetrafluoroethylene (PTFE) to the bottom 34 of expansion layer 18. The PTFE emulsion is dried and then fused at high temperature to provide a well defined PTFE layer 39 which prevents the adhesive layer 38 from bonding to the expansion layer bottom 34.

The PTFE emulsion is preferably an aqueous suspension of very fine PTFE particles. The particle sizes are preferably between about 0.1 to 0.25 microns. The emulsion is preferably applied by silkscreening onto the 25 expansion layer bottom 34. The concentration of PTFE in the aqueous emulsion should be between 55-75 percent by weight depending upon the pore size of the silkscreen used. A PTFE concentration of about 65 weight percent was found to work well when silkscreens having a pore 30 size of 325 mesh are used. The silkscreening process is carried out according to conventional silkscreening techniques which are well known.

Although it is not absolutely necessary, it is preferred that the PTFE particles include a coating of 35 wetting agent to help maintain an aqueous emulsion of the particles. PTFE particles having a wetting agent

coating are available from DuPont Chemical Corp. as TEFLO 120-FEP Dispersion. The identity of the wetting agent used on the TEFLO 120 particles is not known; however, it is believed that any known wetting agent can be used provided that it produces the desired emulsion characteristics and can be evaporated by heating or otherwise removed from the PTFE prior to or during fusion.

As an example of practice, a 65 weight percent aqueous emulsion of TEFLO 120-FEP Dispersion was prepared. The solution was selectively silkscreened onto a flexible polyimide sheet using a 325 mesh silkscreen. The emulsion was dried at 125°C for 30 minutes followed by baking at 500°F (260°C) to remove the coating of wetting agent. The remaining PTFE particles were then fused at 525°F (274°C) to form a solid well-defined layer of PTFE.

The PTFE layer prevents the adhesive layer from bonding to the flexible polyimide sheet at the PTFE layer locations when the flexible sheet is bonded to the circuit board as previously described. The PTFE should be relatively pure. However, minor amounts of impurities or additives are possible provided that the non-bonding characteristics of the PTFE relative to the adhesive layer are not lost.

The PTFE particles may also be selectively applied by spraying or other techniques that can provide the same well-defined surface application provided by silkscreening of aqueous emulsions. Methyl ethyl ketone (MEK) and other suitable solvents can be used for spray application provided that they do not flash off too quickly when the emulsion is sprayed. Acetone does not work well as a solvent or carrier for the PTFE particles for spraying or silkscreening because it flashes off too quickly. The final PTFE layer 39, after fusion, should be as thin as possible while still preventing bonding

between the flexible expansion layer 18 and support layer 20. PTFE layer thicknesses on the order of 0.0001 inch (0.0002 cm) to 0.0003 inch (0.0006 cm) are preferred.

5 The temperature for fusion of the particles should be around 525°F (274°C) or higher. Temperatures above 540°F (282°C) are preferred because it reduces the time required for fusion of the particles into a thin layer. In addition, it should be noted that the PTFE emulsion 10 may be applied to the support layer 28 instead of the expansion layer 18. In either case, the fused PTFE layer will prevent bonding between the expansion layer 18 and support layer 28 when the adhesive is applied. However, it is preferred to apply the PTFE emulsion to 15 the expansion layer 18.

Tests were conducted on leadless ceramic chip carriers (LCCC) as shown in FIGS. 2 and 3 wherein the LCCC size was 84 I/O, 50 mil center. The LCCC's included a polyimide glass printed wiring board (PWB) assembly 20 which was 0.09 inch (0.24 cm) thick. The expansion layer was flexible polyimide sheet made by Enka having a thickness of 0.001 inch (0.002 cm). A vibration test was performed. The purpose of this test was to find out whether any damage would occur under vibration in the 25 following areas: the LCCC solder joint, the thin flexible expansion layer in the unbonded area, and the PWB itself. The test results showed that this PWB could take high vibration input without any damage.

30 Ordinarily, the LCCC solder joints of more rigid PWBs have a better chance for surviving the vibration test because rigid boards have a high resonance frequency. When the PWB is resonant, the solder joints of the LCCC have high stresses. If the natural frequency of the PWB is higher than the electronic system's operating 35 vibration frequency (fans, motors, etc.), the vibration will have a minimum effect on the reliability of the

PWBs. When the PWB is resonant, it vibrates in a wave-form. This waveform tends to pull the PWB away from the LCCC causing high stress on its solder joint.

The compliant-layer PWB of the present invention does not have very high rigidity if no heat sink is used. However, the compliant-layer PWB functions differently from regular PWBs. The thin, flexible, top layer tolerates placement mismatch between the LCCC and the PWB because the thin layer can stretch or compress without creating high stress on the solder joint. This provides a solution to the solder joint failure (due to vibration) of the surface mount device.

Power cycling tests were also performed. All of the compliant-layer PWBs were tested at their worst condition. First, the PWBs were cooled down to -55°C. Then, each LCCC was heated up by chip resistors which were bonded on the LCCCs. The 84-I/O LCCCs used three resistors which dissipated 4.5 watts, the 68-I/O LCCCs used two resistors which dissipated 3 watts, and the 48-I/O LCCCs used one resistor which dissipated 1.5 watts. The PWBs were tested for 1,200 cycles, and none of the solder joints was cracked.

In addition, thermal shock tests were performed. The test procedure was as follows. All of the PWBs were placed into a thermal shock machine. These boards were alternately shifted from a hot chamber to a cold chamber and vice versa. The temperature of the hot chamber was +125°C, and the cold chamber was -55°C. The duration of the PWBs stay in each chamber was 20 minutes.

After a 2,000-cycle thermal shock test, there were no solder joint failures. All of the solder joints locked the same as before the test.

To measure the thermal impedance of the PWBs, the chip resistors were bonded on the center cavity of the LCCCs. It had the same arrangement as the one used for power cycling. The thermocouples were mounted in the

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LCCC cavity on the LCCC wall, and on the PWB. The power consumption of each LCCC and the temperature of each thermocouple were measured. The thermal impedance of the PWB was calculated. The test results showed that 5 the compliant-layer PWB had the same thermal character as the regular polyimide glass PWB.

Having thus described exemplary embodiments of the present invention, it should be noted by those skilled in the art that the within disclosures are exemplary only and that various other alternatives, adaptations and modifications may be made within the scope of the present invention. Accordingly, the present invention is not limited to the specific embodiments as illustrated herein, but are only limited by the following 10 claims.

CLAIMSWhat is Claimed is:

1. A printed wiring board for mounting a ceramic leadless chip carrier, said ceramic leadless chip carrier including a bottom which is attached to the top surface of said printed wiring board, wherein the area on the top surface of said printed wiring board under the location where said ceramic leadless chip carrier bottom is attached thereto defines a chip carrier footprint, and wherein said ceramic leadless chip carrier undergoes expansion and contraction, said printed wiring board comprising:

5 an expansion layer having a bottom surface and a top surface wherein the top surface of said expansion layer forms the top surface of said printed wiring board;

10 a rigid support layer having a bottom and a top surface; and

15 adhesive means located between said expansion layer bottom surface and said support layer top surface for bonding said expansion layer bottom to said support layer top wherein voids are provided in said adhesive means under said chip carrier footprint so that said expansion layer bottom surface is not bonded to said support layer top surface at said chip carrier footprint to thereby allow said expansion layer to expand and contract with said ceramic leadless chip carrier during expansion or contraction thereof irrespective of said support layer.

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3. A printed wiring board according to claim 2 wherein said expansion layer is about 0.0005 inch (0.001 cm) to 0.005 inch (0.013 cm) thick.

4. A printed wiring board according to claim 3 wherein said expansion layer is a flexible polyimide.

5. A printed wiring board according to claim 1 wherein said support layer comprises a plurality of sub-layers laminated together.

6. A printed wiring board according to claim 5 wherein said sub-layers comprise metal, glass, ceramics or rigid plastic.

7. A printed wiring board according to claim 1 wherein said adhesive means comprises an adhesive layer between said expansion layer and said support layer.

8. A printed wiring board according to claim 7 wherein said adhesive layer comprises an adhesive selected from the group consisting of polyimide prepreg and epoxy prepreg.

9. A printed wiring board according to claim 7 wherein said adhesive layer is less than about 0.10 inch (0.25 cm) thick.

10. A printed wiring board according to claim 1 further including a ceramic leadless chip carrier and mounting means for attaching said ceramic leadless chip carrier to the top surface of said expansion layer and wherein expansion and contraction of said expansion layer with the expansion and contraction of said ceramic leadless chip carrier prevents cracking of said mounting means.

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11. A printed wiring board according to claim 1 further including a thin layer of polytetrafluoroethylene located between said expansion layer bottom surface and said printed wiring board top surface at said chip carrier footprint, said layer of polytetrafluoroethylene being positioned so that said adhesive means does not bond to said expansion layer bottom under said chip carrier footprint.

12. A printed wiring board according to claim 11, wherein said thin layer of polytetrafluoroethylene has a thickness of between about 0.0001 inch (0.0002 cm) to 0.0003 inch (0.0006 cm).

13. A method for forming the printed wiring board of claim 11 wherein said thin layer of polytetrafluoroethylene is formed by:

5 applying an aqueous emulsion of polytetrafluoroethylene particles to said expansion layer bottom surface; and

heating said emulsion for a sufficient time and at sufficient temperatures to fuse said polytetrafluoroethylene particles into said thin layer.

14. A method according to claim 13 wherein said aqueous emulsion comprises from 55-75 weight percent polytetrafluoroethylene particles.

15. A method according to claim 14 wherein said polytetrafluoroethylene particles include a surface coating of a wetting agent.

16. A method according to claim 13 wherein the particle size of said polytetrafluoroethylene particles is between about 0.1 micron to 0.25 micron.

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17. A method according to claim 13 wherein said aqueous emulsion of polytetrafluoroethylene particles is selectively applied to said expansion layer bottom surface by silkscreening.

18. A method according to claim 13 wherein said thin layer of fused polytetrafluoroethylene has a thickness of between about 0.0001 inch (0.0002 cm) to 0.0003 inch (0.0006 cm).

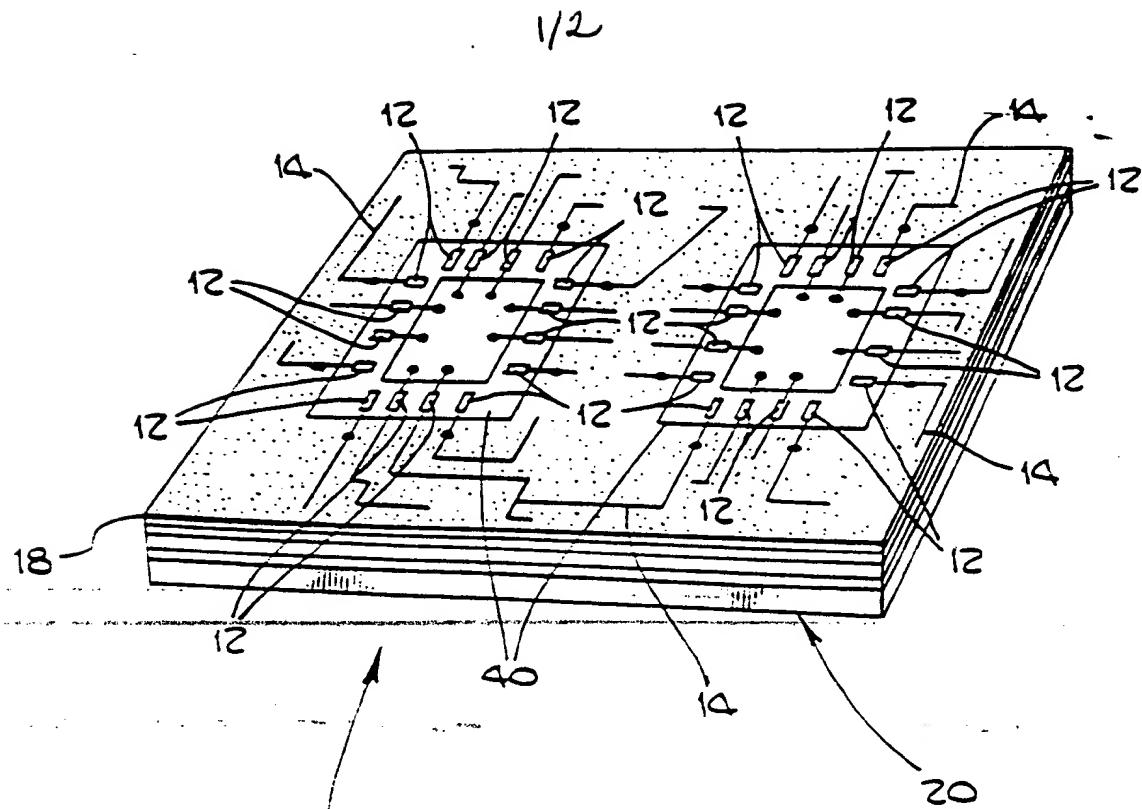
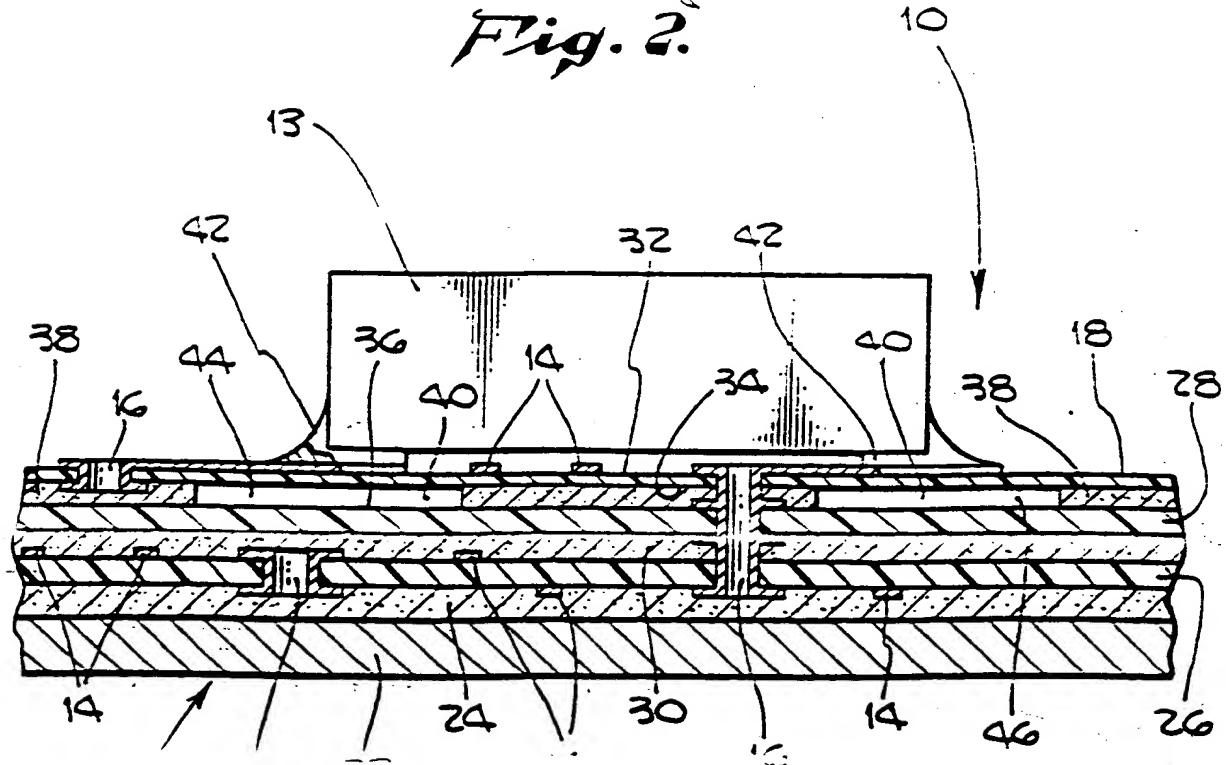
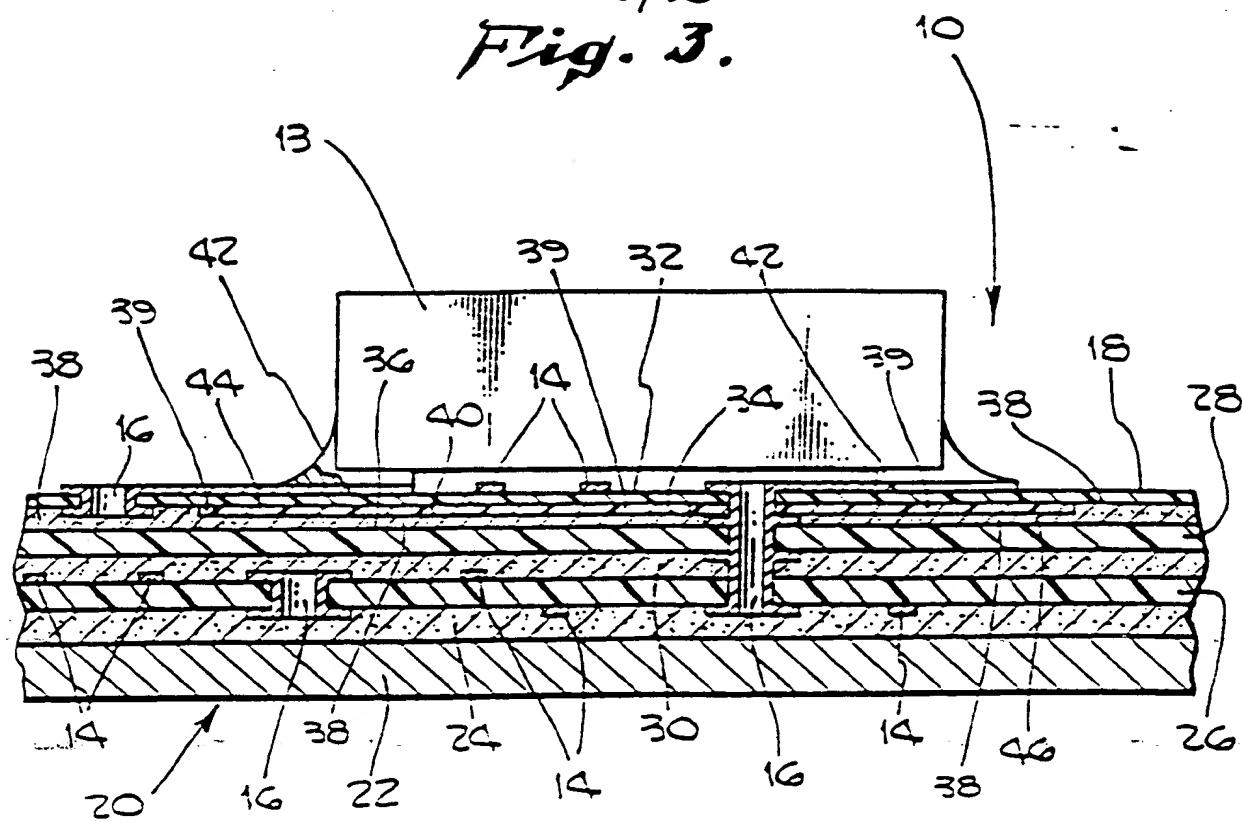


Fig. 1.

Fig. 2.



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Fig. 3.

INTERNATIONAL SEARCH REPORT

TELEGRAM

International Application No.

PCT/US 88/04516

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC⁴: H 05 K 1/18

II. FIELDS SEARCHED

Minimum Documentation Searched *

Classification System	Classification Symbols
IPC ⁴	H 05 K, H 01 L

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched *

III. DOCUMENTS CONSIDERED TO BE RELEVANT*

Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
X	EP, A, 0044247 (SOCAPEX) 20 January 1982 see page 4, line 18 - page 5, line 21; page 6, lines 5-13; page 6, line 14 - page 7, line 19; page 9, line 8 - page 11, line 11; page 13, lines 8-14 --	1-10
A	EP, A, 0075890 (SIEMENS AG) 6 April 1983 --	
A	EDN Electrical Design News, volume 29, no. 17, 23 August 1984, (Boston, Massachusetts, US), R.A. Reynolds: "Clad-metal-core pc boards enhance chip-carrier viability", pages 211-215 -----	

* Special categories of cited documents: to

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"Z" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search

27th June 1989

Date of Mailing of this International Search Report

1 AUG 1989

International Searching Authority

EUROPEAN PATENT OFFICE

Signature of Authorized Officer



P.C.G. VAN DER PUTTEN

36 ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO.

US 8804516

SA 28049

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 25/07/89. The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0044247	20-01-82	FR-A, B 2486755 JP-A- 57042188	15-01-82 09-03-82
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